R16

Code No: 133AJ

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, February -2024

DIGITAL LOGIC DESIGN

(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART- A

(25 Marks)

1.a)	Express the following number in decimal $(10110 . 0101)_2$, $(16 . 5)_{16}$.	[2]
b)	State and prove De Morgan theorems.	[3]
c)	List out the properties of X-OR gates.	[2]
d)	What are prime implicants? Give examples.	[3]
e)	Design a combinational circuit that converts a 4 -bit gray to 4-bit binary code converter.	[2]
f)	Explain the functions of multiplexers and decoders with examples.	[3]
g)	Explain the working of J K Flip – Flop and T – Flip – Flop.	[2]
h)	Design a 4 bit shift register using Flip Flops.	[3]
i)	Write about nature and functions of address bus and data bus.	[2]
j)	Write about sequential memory and Cache memories.	[3]

PART-B

(50 Marks)

2.a) Explain in detail about binary codes, error detecting codes and error correcting codes with examples.

b) Convert the following expression into sum of products and product of sums form
$F = (AB + C)(B + \overline{C} D)$. [5+5]

OR

3.a) Explain the functions of various digital logic gates along with their truth tables.

b) Express the following functions in sum of minterms ad product of maxterms
$F(A,B,C,D) = \overline{B} D + \overline{A} D + BD$. [5+5]

4.a) Explain the simplification of Boolean functions for three variable and four variable with necessary maps.

b) Simplify the Boolean function by first finding the essential prime implicants [5+5]
$F(A,B,C,D) = \sum (1,3,4,5,10,11,12,13,14,15)$.

OR

5.a) Explain the simplification of Boolean functions using sum of products form and product of sums form with examples.

b) Implement the following Boolean function F together with don't care condition using NOR gates $F(A,B,C,D) = \sum (0,1,29,11)$
$d(A,B,C,D) = \sum (8,10,14,15)$. [5+5]

6.a) Explain the analysis procedure for a combinational circuit with help of logic diagram with three inputs and one output. The output is 1. When the binary value of inputs is less than 3. The output is 0 otherwise.

b) Implement the following Boolean function with a multiplexer:
$F(A,B,C,D) = \sum (0,1,3,4,8,9,15)$. [5+5]

OR

7.a) Draw the logic diagram of a 2 to 4 line decoder using NOR gates only. Include an enable input.

b) Construct a 16 × 1 multiplexer with two 8 × 1 and one 2 × 1 multiplexers. Use block diagrams. [5+5]

8.a) Explain the difference among a truth table, a state table a characteristic table and excitation table of a sequential circuit.

b) Draw the logic diagram of a 4 bit binary up/down counter using J – K Flip – Flops. [5+5]

OR

9.a) Show that the characteristic equation for the complement output of a J – K Flip – Flop is $Q^1(t+1) = J^1Q^1 + KQ$.

b) Design a 4 – bit binary synchronous counter with D – Flip – Flops. [5+5]

10.a) Explain the features of various memories used in digital logic design and draw the internal logic diagram of a 32 × 8 ROM.

b) Implement the following two Boolean functions with a PLA
$F_1(A, B, C) = \sum (0, 1, 2, 4)$
$F_2(A, B, C) = \sum (0, 5, 6, 7)$. [5+5]

OR

11.a) Discuss various types of ROMs and combinational programmable logic devices with basic Configurations.

b) Design a combinational circuit using a ROM which accepts a 3 – bit number and generates an output binary number equal to the square of the input number. [5+5]

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